In the Claims

Please rewrite claims 1 and 23 as follows:

1. (Amended) A charge pump circuit comprising:

a first plurality of serially connected transistors of a first conductivity type;

a second plurality of serially connected transistors of a second conductivity type;

said first plurality of serially connected transistors being serially connected to the second plurality of serially connected transistors;

the interconnection of said first and second plurality of transistors providing an output;

a gate of one of said first plurality of transistors being adapted to receive a $\overline{\text{DOWN}}$ pulse signal, a gate of another one of said first plurality of transistors being adapted to receive a DC bias signal, a gate of one of said second plurality of transistors being adapted to receive an UP pulse signal, and a gate of another one of said second plurality of transistors being adapted to receive another DC bias signal; and

a first node at the interconnection of transistors of said first plurality of transistors being adapted to receive a DOWN pulse signal and a second node at the interconnection of transistors of said second plurality of transistors being adapted to receive an $\overline{\text{UP}}$ pulse signal.

23. (Amended) A method of operating a charge pump comprising:

switching a first switching transistor in response to a first applied switching signal to affect an output at an output terminal;

switching a second switching transistor in response to a second applied switching signal to affect an output at said output terminal;

biasing the switching characteristics of said first and second switching transistors with bias transistors respectively serially connected to said first and second switching transistors;

coupling a complementary signal of said first applied switching signal to a connection between said first switching transistor and an associated bias transistor; and

coupling a complementary signal of said second applied switching signal to a connection between said second switching transistor and an associated bias transistor to maintain a substantially continuously controlled voltage at said output terminal.